What is claimed is:

1. A data processing system for manipulating data, comprising; an integrated circuit data flow processor, said data flow processor comprising a plurality of logically and structurally identical cells arranged orthogonal relative to one another, a plurality of connecting lines disposed between each said cells and a plurality of input and output ports, said cells connected to neighboring cells by a plurality of first data connections, said cells also connected to said connecting lines by a plurality of second data connections, said cells capable of being combined and facultatively grouped into functional parts by means of said first and second data connections, said cells connected to said input and output ports; a compiler capable of programming and configuring said cells and facultatively grouping said cells into functional parts such that various logic functions and data manipulations among said cells and said functional parts can be realized, said compiler capable of manipulating said cells and said functional parts during operation of said data flow processor such that portions of the data flow processor not being manipulated are not halted or impaired in their operation.

2. The data processing system according to Claim 1, further comprising a memory, wherein said memory is coupled with said compiler and said memory is adapted to specify the configuration of said cells.

3. The data processing system according to Claim 2, wherein said compiler manages a program sequence based on data and programs stored in separate memories, in the sense of a Harvard structure.

4. The data processing system according to Claim 3, wherein said compiler comprises logically and structurally identical cells.

5. The data processing system according to Claim 4, wherein said compiler is adapted to dynamically reconfigure said data flow processor during a program sequence during operation of said data processing system, without influencing the data to be processed.

6. The data processing system according to Claim 1, wherein said compiler manages a program sequence based on data and programs stored in separate memories, in the sense of a Harvard structure.

7. The data processing system according to Claim 6, wherein said compiler comprises logically and structurally identical cells.

8. The data processing system according to Claim 7, wherein said compiler is adapted to dynamically reconfigure said data flow processor during a program sequence during operation of said data processing system, without influencing the data to be processed.

9. The data processing system according to Claim 1, wherein said compiler is adapted to dynamically reconfigure said data flow processor during a program sequence during operation of said data processing system, without influencing the data to be processed.

10. The data processing system according to Claim 1, wherein said data flow processor is configured to be capable of coordinating a plurality of data in

put/output units and a plurality of memory units such that said data processing system operates as a highly complex and complete computer system.

11. The data processing system according to Claim 10, wherein some functions of said data input/output units are capable of being implemented on said data flow processor.

12. A data processing system for manipulating data, comprising; an integrated circuit data flow processor, said data flow processor comprising a plurality of logically and structurally identical cells arranged orthogonal relative to one another, a plurality of connecting lines disposed between each said cells and a plurality of input and output ports, said cells connected to neighboring cells by a plurality of first data connections, said cells also connected to said connecting lines by a plurality of second data connections, said cells capable of being combined and facultatively grouped into functional parts by means of said first and second data connections, said cells connected to said input and output ports, said cells capable of being programmed and configured to be facultatively grouped into functional parts such that various logic functions and data manipulations among said cells and said functional parts can be realized, wherein a plurality of said data flow processors are coupled in cascade form.

13. The data processing system according to Claim 12, wherein said data flow processor is configured to be capable of coordinating a plurality of data input/output units and a plurality of memory units such that said data processing system operates as a highly complex and complete computer system.

14. The data processing system according to Claim 13, wherein some functions of said data input/output units are capable of being implemented on said data flow processor.